ABSTRACT

A memory cell comprises a chalcogenide random access memory (CRAM) cell and a CMOS circuit. The CMOS circuit accesses the CRAM cell. The CRAM cell has a cross-sectional area that is determined by a thin film process (e.g., a chalcogenide deposition thin film process) and by an iso-etching process. If desired, the chalcogenide structure may be implemented in series with a semiconductor device such as a diode or a selecting transistor. The diode drives a current through the chalcogenide structure. The selecting transistor drives a current through the chalcogenide structure when enabled by a voltage at a gate terminal of the selecting transistor. The selecting transistor has a gate terminal, a source terminal, and a drain terminal; the gate terminal may be operatively coupled to a word line of a memory array, the source terminal may be operatively coupled to a drive line of the memory array, and the drain terminal may be operatively coupled to a bit line of the memory array.